IN THE SPECIFICATION

At page 1, line 2 insert the following: The present application is a divisional of U.S. Patent Application No. 10/071,581, filed February 7, 2002, entitled "INTEGRATED PASSIVE COMPONENTS AND PACKAGE WITH POSTS," which is a divisional of U.S. Patent Application No. 08/855,105, filed May 13, 1997, which issued as U.S. Patent No. 6,414,585 B1 on July 2, 2002. This application claims priority from both U.S. Patent Application Nos. 10/071,581 and 08/855,105.

Please amend the paragraph at page 1, line 23 of the application as follows:

One prior art method of solving the problems of wire bonds is the flip chip. ~~Figure 1~~ Figures 1A and 1B ~~illustrates~~ illustrate a prior art electronic component that is packaged as a flip chip. The flip chip 110 includes an integrated circuit 120 (IC) and solder balls 140 attached to the IC 120. The IC 120 is a conventional integrated circuit, which has contact points, to which solder balls 140 are attached. The flip chip 110 is placed on a substrate 150 which includes a plurality of contact pads. The solder balls 140 of flip chip 110 are reflowed to attach the flip chip 110 to the contact pads on the substrate. In order to prevent solder joint failure caused by coefficient of thermal expansion (CTE) mismatch between substrate 150 and flip chip 110, the area between the solder balls 140 is filled with an underfill 130. The underfill 130 is injected between the IC 120 and the substrate 150. The underfill 130, substrate 150, IC 120 and solder balls 140 form a single unit.

Please amend the paragraph at page 4, line 6 of the application as follows:

Another object of the present invention is to provide an encapsulation of the package in order to provide protect to the circuit.

Please amend the paragraph at page 5, line 5 of the application as follows:

~~Figure 1 illustrates~~ Figures 1A and 1B illustrate a prior art integrated circuit that is packaged as a flip chip.

Please amend the paragraph at page 5, line 9 of the application as follows:

~~Figure 3 illustrates~~ Figures 3A and 3B illustrate a die. The electric component has a first side 322, a second side 324, a top 326, and a bottom 328.

Please amend the paragraph at page 5, line 10 of the application as follows:

~~Figure 4 illustrates~~ Figures 4A and 4B illustrate the die with a first passivation layer.

Please amend the paragraph at page 5, line 11 of the application as follows:

~~Figure 5 illustrates~~ Figures 5A and 5B illustrate the die with metal beams.

Please amend the paragraph at page 5, line 12 of the application as follows:

~~Figure 6 illustrates~~ Figures 6A and 6B illustrate the die with a second passivation layer.

Please amend the paragraph at page 5, line 13 of the application as follows:

~~Figure 7 illustrates~~ Figures 7A and 7B illustrate the die with a cap.

Please amend the paragraph at page 5, line 14 of the application as follows:

~~Figure 8 illustrates~~ Figures 8A and 8B illustrate the die with a thin cap.

Please amend the paragraph at page 5, line 15 of the application as follows:

~~Figure 9 illustrates~~ Figures 9A and 9B illustrate the die with trenches.

Please amend the paragraph at page 5, line 16 of the application as follows:

~~Figure 10 illustrates~~ Figures 10A and 10B illustrate the die with a third passivation layer.

Please amend the paragraph at page 5, line 17 of the application as follows:

~~Figure 11 illustrates~~ Figures 11A and 11B illustrate the die with layers over the contact points etched away, exposing contacts.

Please amend the paragraph at page 5, line 19 of the application as follows:

~~Figure 12 illustrates~~ Figures 12A and 12B illustrate the die with a conductive layer.

Please amend the paragraph at page 5, line 20 of the application as follows:

~~Figure 13 illustrates~~ Figures 13A and 13B illustrate the die with a coating layer.

Please amend the paragraph at page 5, line 21 of the application as follows:

~~Figure 14 illustrates~~ Figures 14A and 14B illustrate the dies with an encapsulant on the backside of the circuit.

Please amend the paragraph at page 5, line 23 of the application as follows:

~~Figure 15 illustrates~~ Figures 15A, 15B, and 15C illustrate a circuit with the active side of the substrate processed according to the present invention.

Please amend the paragraph at page 6, line 1 of the application as follows:

~~Figure 16 illustrates~~ Figures 16A, 16B, and 16C illustrate the circuit of ~~Figure 15~~ Figures 15A, 15B, and 15C with a trench on the back side.

Please amend the paragraph at page 6, line 3 of the application as follows:

~~Figure 17 illustrates~~ Figures 17A, 17B, and 17C illustrate the circuit of ~~Figure 16~~ Figures 16A, 16B, and 16C with a metal layer deposited over the back side of the circuit.

Please amend the paragraph at page 6, line 5 of the application as follows:

~~Figure 18 illustrates~~ Figures 18A, 18B, and 18C illustrate the circuit of ~~Figure 17~~ Figures 17A, 17B, and 17C with an encapsulant covering the back side of the circuit.

Please amend the paragraph at page 6, line 11 of the application as follows:

~~Figure 21 illustrates~~ Figures 21A and 21B illustrate a resistor implemented on a substrate according to the present invention.

Please amend the paragraph at page 6, line 13 of the application as follows:

~~Figure 22 illustrates~~ Figures 22A and 22B illustrate a capacitor implemented on a substrate according to the present invention.

Please amend the paragraph at page 6, line 15 of the application as follows:

~~Figure 23 illustrates~~ Figure 23A and 23B illustrate an inductor implemented on a substrate according to the present invention.

Please amend the paragraph at page 6, line 17 of the application as follows:

~~Figure 24 illustrates~~ Figures 24A and 24B illustrate a diode implemented on a substrate according to the present invention.

Please amend the paragraph at page 7, line 3 of the application as follows:

~~Figure 2 illustrates~~ Figures 2A and 2B illustrate a wafer with which embodiments of the present invention may be implemented. Wafer 210 is an electronic component wafer containing a fully processed electronic component. The electronic component can include an integrated circuit, an integrated passive network, or a discrete component. Wafers of various sizes may be used. One area 220 of the wafer 210 is expanded for a better image. The area 220 contains one electronic component 230, which is delineated in ~~Figure 2~~ Figures 2A and 2B by dashed lines. In actual

implementation, no such lines are visible. The electronic component 230 contains a plurality of contact pads 240. Such contact pads are ~~be~~ made of a metal, such as aluminum. Further processing steps illustrate the electronic component 230 as it is processed.

Please amend the paragraph at page 7, line 3 of the application as follows:

Figures ~~3-13~~ 3A-13B show the processing of an electronic component. For one embodiment the processing illustrated below occurs at a wafer level prior to the separation of the wafer into individual dies. Wafer level packaging is advantageous because it permits processing to occur simultaneously for multiple dies, and does not require individual handling of the dies. Furthermore, because the dies are prepared in the same process, uniformity of processing is assured. The figures below illustrate a single die, however, it is understood that the processing is wafer level, and occurs to all dies on the wafer substantially simultaneously.

Please amend the paragraph at page 7, line 24 of the application as follows:

~~Figure 3 illustrates~~ Figures 3A and 3B illustrate an electronic component die. For one embodiment, the electronic component is an integrated circuit, an electronic circuit, an active discrete electronic component, a passive discrete electronic component, or ~~an other~~another similar device. The die 310 is a processed electronic component with a plurality of contact points 320 on a substrate. The substrate may be silicon, gallium-arsenide, silicon germanium, silicon carbide, gallium phosphide, ceramic materials, sapphire, quartz, or other substrate materials. The contact points are bonding pads, or similar sites. For one embodiment, the contact points 320 are aluminum. Alternatively, the contact points 320 are ~~be~~ any conductive materials.

Please amend the paragraph at page 8, line 9 of the application as follows:

~~Figure 4 illustrates~~ Figures 4A and 4B illustrate a die with a first passivation layer 410. The passivation layer 410 is deposited by spinning, vapor deposition, or other known methods. For one embodiment, the passivation layer 410 is polyimide. Alternatively, the passivation layer 410 is made of silicon nitride, silicon dioxide, epoxy, plastic, resin, Teflon, silicon oxide, silicon, polysilicon, amorphous silicon, aluminum, diamond, or other insulating material. The entire circuit is covered by passivation layer 410. Alternatively, the passivation layer 410 is removed from the contact points 320 by etching. Alternatively, the passivation layer 410 is deposited using masking, ~~and~~ which leaves the contact points 320 exposed. For one embodiment, the present packaging process starts at this point. The first passivation layer 410 is deposited during the formation of the electronic component.

Please amend the paragraph at page 8, line 21 of the application as follows:

~~Figure 5 illustrates~~ Figures 5A and 5B illustrate a die with metal beams 510. Metal beams 510 are deposited over the passivation layer 410, and are in electrical contact with contact points 320. For one embodiment, a barrier metal such as titanium tungsten/gold (TiW/Au) is first sputter deposited over the entire circuit. The barrier metal provides a barrier layer between metals and enhances adhesion of the metal beams 510. After the deposition of the metal beams 510, the barrier metal layer is etched away from the remaining areas of the electronic component 300. The metal beams 510 are deposited in order to lead the contact points 310 to a location adjacent to the position where a post is deposited, as will be described below. If the contact points 310 are in the correct position, this step may be omitted. The metal beams 510

are made of gold, silver, nickel, titanium, aluminum, copper, platinum, or ~~an other~~ another conductive metal. For one embodiment, the metal beams 510 extend to the edge of the electronic component. For one embodiment, metal beams 510 are 4-8 microns in thickness.

Please amend the paragraph at page 9, line 11 of the application as follows:

~~Figure 6 illustrates~~ Figures 6A and 6B illustrate a die with a second insulating layer 610. The second insulating layer 610 is deposited over the passivation layer 410 and the metal beams 510. For one embodiment, the insulating layer 610 is a polyimide layer, and is deposited by spinning. Alternatively, the second insulating layer 610 may be made of any of the materials listed for the passivation layer 410. For one embodiment, the insulating layer 620 covers the entire electronic component 300. For another embodiment, the insulating layer 610 is not deposited over all of the metal beams 510. Rather, some part of the metal beams 620 remain uncovered. Alternatively, insulating layer 610 is deposited over the entire electronic component and etched from part of the metal beams 620. For one embodiment a wet etch is used to etch away the insulating layer 610. Alternatively, a dry etch is used.

Please amend the paragraph at page 9, line 23 of the application as follows:

~~Figure 7 illustrates~~ Figures 7A and 7B illustrate the die with a cap 710. The cap 710 is attached to the electronic component 300 and covers the entire electronic component 300. For one embodiment, the electronic component is covered with an insulating layer 740, and the bottom of the cap 710 is covered with another insulating layer 730. For one embodiment, the two insulating layers 730, 740 are partially cured. Such partial curing strengthens the insulating layers 730, 740 and makes the insulating

layers 730, 740 more resistant to acid etching. The partial curing is accomplished by heating, irradiating with an ultraviolet light, or similar techniques. The technique used for curing depends on the material being used for insulation. After partial curing, the cap 710 covered with insulating layer 730 is placed on top of the electronic component 300 covered with insulating layer 740, and joined together. The insulating layers 730 and 740 act as a glue, and together from the gluing layer 750. Alternatively, the cap 710 is grown or sputter deposited.

Please amend the paragraph at page 10, line 12 of the application as follows:

~~Figure 8 illustrates~~ Figure 8A and 8B illustrate the die with a thin cap 810. The cap 710 is thinned to form a thin cap 810. For one embodiment, the cap 710 is sandblasted and etched. Alternatively, the cap 710 is thinned by grinding, etching, or other known techniques. The resulting thin cap 810 is approximately 3-15 thousandth of an inch (mil) in height, depending on compliancy and standoff required. Alternatively, the original cap 710 may be sufficiently thin not to require this step. Alternatively, this step is omitted.

Please amend the paragraph at page 10, line 19 of the application as follows:

~~Figure 9 illustrates~~ Figures 9A and 9B illustrate the cap 810 with trenches 930. The thin cap 810 is patterned. For one embodiment, patterning is accomplished using a wet etch. The trenches 930 define posts 910 and a central area 920. The thin cap 810 is etched away at these trenches 930 to the gluing layer 750. The trenches 930 are located such that they expose the gluing layer 750 over the contact areas 310 or metal beam 510. For one embodiment, the posts 910 are approximately 4 mils by 4 mils in size at their narrowest. The size of the posts 910 is limited by the minimum

working size of the equipment used, and the stability requirement of the circuit. For one embodiment, the base size of posts 910 is maximized in order to assure proper adherence and stability. The trenches 930 are approximately 8 mils in width, and are etched around each of the posts 910. Thus, the remaining area of the circuit is covered by the central area 920. Alternatively, the central area 920 is etched away, leaving only posts 910. For one embodiment, posts 910 are 4-6 mils in thickness.

Please amend the paragraph at page 11, line 8 of the application as follows:

Figures ~~7-9~~ 7A-9B illustrate one method of forming the posts 910 used in the present invention. Alternative methods include photoforming posts 910 from an encapsulated material. Such a material would provide additional compliancy inherent in the posts 910. Alternatively, the posts 910 are a material such as plastic, metal, or other material described above with respect to the cap 710. For one embodiment, a material with compliancy is used to form the posts 910. Such posts 910 may either be formed as described above, grown, prefabricated, and attached, stenciled, or made by other means known in the art. For one embodiment, the posts 910 are made of silicon, gallium arsenide, silicon germanium, silicon carbide, gallium phosphide, ceramic materials, sapphire, quartz, or other substrate materials. Alternatively, the posts 910 are made of polymer plastic, patterned plastic, epoxy, glass, Teflon, silicon dioxide, polysilicon, or any other material which can provide mechanical support for the conductive layer described below. The result is posts 910 which are positioned adjacent to metal beams 510 or contact points 320.

Please amend the paragraph at page 11, line 24 of the application as follows:

~~Figure 10 illustrates~~ Figures 10A and 10B illustrate the die with third insulating layer 1010. The third insulating layer 1010 is deposited over the entire electronic component ~~300~~, covering the trenches. The overlaying insulating layer 1010 is for keeping the posts 910 in place and providing further compliancy. For one embodiment, third insulating layer 1010 is a polyimide layer, which is deposited by spinning. For one embodiment, this step is omitted.

Please amend the paragraph at page 12, line 5 of the application as follows:

~~Figure 11 illustrates~~ Figures 11A and 11b illustrate the die with the layers over the contact points ~~320~~ removed, exposing contacts 1110. Contacts 1110 may be contact points 320 or metal beams 510. The hole is etched through the layers which may include insulating layer 1010 and the gluing layer 750, to the underlying metal. For one embodiment, this is accomplished using photo imaging to remove insulating layer 1010, and a dry etch to remove gluing layer 750.

Please amend the paragraph at page 12, line 11 of the application as follows:

~~Figure 12 illustrates~~ Figures 12A and 12B illustrate the die with a conductive layer 1210. The conductive layer 1210 is deposited on the posts ~~910~~ and the exposed portions of contacts 1110. For one embodiment, prior to depositing the conductive layer 1210 a barrier metal such as titanium tungsten/gold (TiW/Au) is first sputter deposited over the entire circuit. The barrier metal provides a barrier layer between metals and enhances adhesion of the conductive layer 1210. After the deposition of conductive layer 1210, the barrier metal layer is etched away from the remaining areas of the electronic component.

Please amend the paragraph at page 12, line 19 of the application as follows:

For one embodiment, the conductive layer 1210 comprises a first gold layer 1230, a nickel layer 1240 and a flash gold layer 1250. For one embodiment, the nickel layer 1240 is deposited using electroless deposition, i.e. by chemical reduction. For one embodiment, the first gold layer 1230 is 4-8 microns and the nickel layer 1240 is 4-6 microns in thickness. The nickel layer 1240 is used because the gold layer 1230 should not be in contact with solder because it might affect solder joint reliability. The nickel layer 1240, however, is susceptible to oxidization. To avoid oxidization, for one embodiment, a flash gold layer 1250 is deposited over the nickel layer ~~1250~~1240. The conductive layer 1210 may further be deposited on the central area ~~920~~, in order to use the central area 920 as a hest sink. Alternatively, the central area 920 is covered with a different metal, such as nickel and a layer of flash gold, or left without a metal coating layer.

Please amend the paragraph at page 13, line 7 of the application as follows:

~~Figure 13 illustrates~~ Figure 13A and 13B illustrate the die with a coating layer 1310. The coating layer 1310 is used to cover the metal beams ~~620~~, protect the electronic component 310, and to cover the electrically conductive areas of the circuit. For one embodiment, the coating layer 1310 is not deposited on the top of posts ~~910~~ and the top of central area 920. Thus the metallized top of the posts 910 remains electrically conductive. The coating layer 1310 is deposited using a masking process. Alternatively, the coating layer 1310 is deposited uniformly over the entire circuit, and removed from the top of the posts910 and central area 920 using photo imaging techniques. For one embodiment, the coating layer 1310 is an encapsulant, which is polyimide. Alternatively, the coating layer 1310 is an epoxy.

Please amend the paragraph at page 13, line 18 of the application as follows:

~~Figure 14 illustrates~~ Figures 14A and 14B illustrate the die with an encapsulant. The backside of electronic component ~~300~~ is exposed, and there is a danger that the backside of the silicon may become chipped or otherwise damaged. An encapsulant 1410 is used to prevent such an occurrence. For one embodiment, the encapsulant 1410 is epoxy. Alternatively, other materials may be used. For one embodiment, the area between the individual dies is sawed partially prior to the deposition of the encapsulant 1410. This allows the encapsulant to cover the sides as well as the backside of the electronic component.

Please amend the paragraph at page 14, line 1 of the application as follows:

~~Figure 15 illustrates~~ Figures 15A, 15B, and 15C illustrate a circuit, and part of an area adjacent to the circuit 1510. Circuit 1510 is processed according to the process described above with respect to Figures ~~3-14~~3A-14B. The top view 1510 shows the conductive layer 1580 over posts 1520. The trenches 1540 between the posts 1520 are coated with an encapsulant 1550 which holds posts 1520 in place, and protects the conductive areas from the accidental short circuits. The conductive layer 1580 on posts 1520 is in contact with metal beam 1570, which is in electrical contact with contact area 1530 on the surface of the electronic component. There may also be metal beams 1575 which are not in contact with any contact areas 1530 on the electronic component. For one embodiment, metal beams 1570, 1575 extend beyond the end of circuit 1510 by approximately 3-12 mil. For one embodiment, there is approximately 10 mil between each circuit on the wafer. In these 10 mil, there are no underlying active areas. The back side 1560 of the semiconductor substrate is thin. For one

embodiment, the back side 1560 of the semiconductor substrate is thinned to 3-10 mils. Generally, a semiconductor substrate 1590 is relatively thick but only has active components on or near the surface. The thickness of the substrate 1590 simplifies processing. The semiconductor substrate 1590 is thinned by sandblasting, grinding, etching, or other known techniques. The etched back side 1560 of semiconductor 1590 is a relatively flat semiconductor 1590 is a relatively flat semiconductor surface.

Please amend the paragraph at page 14, line 21 of the application as follows:

~~Figure 16 illustrates~~ Figures 16A, 16B, and 16C illustrate the circuit of ~~Figure 15~~ Figures 15A, 15B, and 15C with a trench 1620. The trench is placed between the electronic components, substantially under a metal beam 1575. The metal beam 1575, which is over the trench 1620, is not in electrical contact with any contact areas 1530. For one embodiment, the trench 1620 is created in a two step process. First, a saw blade is used to saw down almost to the metal beam 1575. For one embodiment, the saw blade is 2 or 4 mil blade. Then, this sawed out portion is further etched, to extend the trench 1620 to the metal beam 1575. The etch, which is a wet etch, widens and deepens the trench 1620. For one embodiment, the trench 1620 is approximately 3-8 mil in width, and the bottom 1630 of the trench 1620 is approximately 1-3 mils from the end of the post 1520. For one embodiment, the step of sawing out is skipped if the etch used is sufficiently precise to form trench 1620. The sawing out makes the etch more precise and directed.

Please amend the paragraph at page 15, line 9 of the application as follows:

~~Figure 17 illustrates~~ Figures 17A, 17B, and 17C illustrate the circuit of ~~Figure 16~~ Figures 16A, 16B, and 16C with a metal layer 1720 deposited over the bottom 1630 of

the circuit. For one embodiment, the metal layer 1720 covers the entire back side 1560 of the circuit. Alternatively, metal layer 1720 may cover only part of the back side 1560 of the circuit. The metal layer 1720 is in electrical contact with at least one metal beam 1575. For one embodiment, metal layer 1720 only contacts some of the metal beams 1570, 1575. Specifically, only those metal beams 1575 which act as ground are electrically coupled to the metal layer 1720. Additionally, the metal layer 1720 may act as a drain in circuits which use a drain. Metal layer 1720 may further act as a heat sink. For one embodiment, metal layer 1720 is a plated nickel layer. For one embodiment, the metal layer 1720 is further covered with a flash gold layer, to prevent oxidization.

Please amend the paragraph at page 15, line 21 of the application as follows:

~~Figure 18 illustrates~~ Figures 18A, 18B, and 18C illustrate the circuit of ~~Figure 17~~ Figures 17A, 17B, and 17C with an encapsulant 1820 covering the ~~back side 1560~~ backside of the circuit. For one embodiment, encapsulant 1820 is an epoxy. For one embodiment, prior to the deposition of encapsulant 1820 a thick blade is used to saw the side of the circuit without the trench. The thick saw blade, for one embodiment, a 6 mil blade, creates a slot 1830 which is then covered with encapsulant 1820. The encapsulant 1820 covers the back side 1560 and part of the sides of the electronic component, protecting if from the environment and further processing. Encapsulant 1820 also covers trench 1620 and slot 1830, such that back side 1560 of the circuit is substantially flat. This simplifies further handling of the circuit, and makes it more robust.

Please amend the paragraph at page 16, line 7 of the application as follows:

For one embodiment the processing illustrated in Figures ~~15-18~~15A-18C may be accomplished prior to the forming the posts on the active side of the substrate. In this way, the danger of damaging the posts or the conductive layer on the posts are minimized. For simplicity's sake, in this example, the active side and back side processes were separated.

Please amend the paragraph at page 19, line 13 of the application as follows:

~~Figure 21 illustrates~~ Figures 21A and 21B illustrate a resistor implemented on a substrate according to the present invention. A substrate 2110 is silicon, or any other known substrate material. A passivation layer 2115 is deposited over the substrate. The passivation layer 2115 is the insulating layer described with respect to ~~Figure 5~~ Figures 5A and 5B.

Please amend the paragraph at page 20, line 20 of the application as follows:

~~Figure 22 illustrates~~ Figures 22A and 22B illustrate a capacitor implemented on a substrate 2210 according to the present invention. A passivation layer 2215 is deposited on a substrate 2210. The substrate 2210 may contain other electronic components. The capacitor of the present invention is not deposited over any contact areas which are part of the electronic component. A thin film 2220 is deposited over the passivation layer 2215. The thin film 2220 is one of the plates which form a capacitor. A contact area 2225 is designated on the thin film 2220. An insulating layer 2230 overlays ~~he~~ the metal layer 2220 and passivation layer 2215, but leaves the contact area 2225 exposed. The insulating layer 2230 acts as a dielectric for the capacitor.

Please amend the paragraph at page 21, line 21 of the application as follows:

~~Figure 23 illustrates~~ Figures 23A and 23B illustrate an inductor implemented on a substrate according to the present invention. A passivation layer 2320 is deposited over a substrate 2310. An insulating layer 2330 is deposited over the passivation layer 2320. An inside post 2360 and an outside post 2370 overlay the insulating layer 2330. A conductive layer 2350 is deposited over the top of the posts 2360, 2370. The conductive layer 2350 is further deposited as a patterned conductive layer 2355 on the insulating layer 2330. For one embodiment, patterned conductive layer 2355 is deposited on a spiral pattern, extending from a central post 2360 to an outside post 2370. The spiral pattern induces inductance in the patterned conductive layer 2355. Thus, the shape of the pattern of the patterned conductive layer 2355 is designed to have the inductance required. The area between the post 2360, 2370 is covered with a fixing passivation layer 2380, which is an encapsulant such as polyimide. The fixing passivation layer 2380 is for keeping the posts 2360, 2370 in place and isolating the patterned conductive layer 2355 and conductive layer 2350 on the sides of posts 2360, 2370. A contact layer 2390 may further be deposited on the conductive layer 2380 on top of posts 2360, 2370. The contact layer 2390, which is at the top of the posts 2235, ~~are~~ is placed in contact with a printed circuit board.

Please amend the paragraph at page 22, line 15 of the application as follows:

~~Figure 24 illustrates~~ Figures 24A and 24B illustrate a diode implemented on a substrate according to the present invention. The substrate 2410 has a PN junction 2415 embedded in it. The PN junction 2415 is created using conventional processes. A contact area 2420 is defined. One of the contact areas 2420 is in contact with the PN junction 2415. ~~An~~A passivation layer 2425 is deposited over the circuit, leaving the

contact areas 2420 exposed. An insulating layer 2430 is deposited over the circuit, leaving the contact areas 2420 exposed. Alternatively, both insulating layer 2430 and passivation layer 2425 is etched to expose contact areas 2420.